INDUCTORLESS MONOLITHIC MICROWAVE AMPLIFIERS WITH DIRECTLY CASCADED CELLS

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Abstract—**Design and performance of inductorless cascadable amplifier cells are described. Using an $f_T = 15$ GHz GaAs FET MMIC process [1], broadband cells employing a new "additive gain" technique are directly cascaded to form a 26 dB-gain, 80 MHz - 4.5 GHz amplifier. A multistage narrowband design exhibits 25 dB gain at 3.5 GHz with 1.6 GHz bandwidth. A compact FET synthetic inductor is compared to square spiral inductors for these designs.**

I. INTRODUCTION

Many circuit design techniques can be used to increase broadband amplifier bandwidth within a particular MMIC process. The feedback technique [2], and the inductive gain-peaking technique [6] are two examples. High-gain is achieved by cascading two or more stages [2]-[5]. However, when a multistage amplifier is formed with each stage containing inductive peaking elements (generally spiral inductors), the size of the circuit becomes a critical issue in reducing process variation and cost.

This paper describes three-stage direct-coupled amplifiers (both wideband and narrowband) using synthetic inductors as alternative peaking elements over the more conventional spiral inductors. These amplifiers are completely self-biasing and requires +6 volt and -4 volt power supplies for operation.

II. THE CASCADABLE CELL

The basic amplifier cell reported here utilizes a common-source MESFET with a resistor-inductor load, as shown in Fig. 1(a). This portion of amplifier is referred to as the "inverter"; it exhibits gain peaking when capacitively loaded. The voltage gain of the inverter is given by:

$$A_V = \frac{-g_m R(1+sL/R)}{s^2LC+sRC+1}$$

where g_m is FET transconductance, and "s" denotes complex frequency variable.

The pole frequencies are determined by the quadratic equation solution:

$$s_p = -\frac{R}{2L} \pm j\sqrt{\frac{1}{LC}-\frac{R^2}{4L^2}}$$

As the ratio of imaginary part to real part increases, the gain peaking becomes more pronounced.

However, a limit on the gain peaking is set by the practical inductors that are realizable in monolithic circuits and the amount of capacitive loading imposed by the gate capacitance of the succeeding stage.

A buffer circuit, as shown in Fig. 1(b), can be used to reduce capacitive loading presented to the inverter, and to introduce a low-Q inductive output impedance to capacitive loads. The inverter and buffer circuits are connected as shown in Fig.2 to form a single-cell *cascadable amplifier*.

Both narrowband and wideband amplifiers can be designed depending on the signal path(s) formed. The amplifier cell shown in Fig. 2(a) has a single signal path (I) through the inverter and the non-inverting buffer input. When the resistive component of the inverter load is chosen such that $g_{m,input\ FET} \cdot R = 1$, a band-pass characteristics results; it displays near-unity low frequency gain which peaks at higher frequencies due to resonance between the inductive element and buffered load capacitance.

When the signal path (I) is severed and the gates of input and output FETs are connected together [Fig. 2(b)], the signal follows the path (II). The source follower's gate is effectively ac grounded. This circuit functions as a unity-gain inverter which rolls off at higher frequencies due to capacitive loading.

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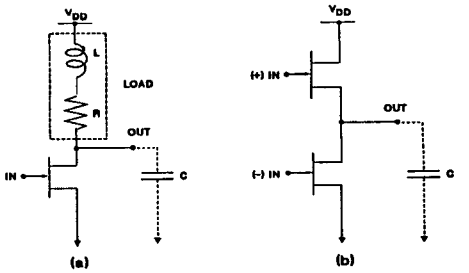


Fig. 1. Elements of cascadable amplifier cells (a) An inverting amplifier stage with near-unity low frequency gain inductively peaked at high frequencies (b) A buffer stage that has near-unity gain through each input (+ or -), and a gain of approximately two when operated push-pull.

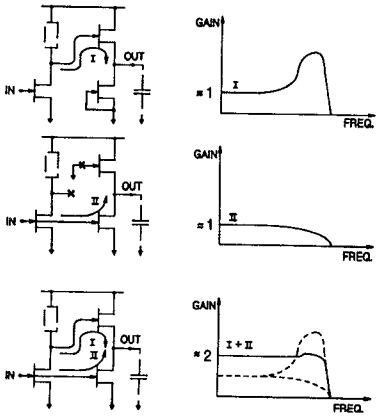


Fig. 2. Cascadable Cells. (a) A narrowband amplifier cell with near-unity low frequency gain and resonant gain peaking at high frequencies. (b) An inverter with near-unity gain and lower frequency roll-off due to the absence of peaking inductor. (c) An additive-gain cell which sums signals from paths (I+II) at the output, producing gain=2 with flat frequency response.

The additive-gain amplifier cell is constructed by combining the two signal, (I) and (II), as shown in Fig. 2(c). The signal amplification takes place through paths (I) and (II), which are summed at the output. This cell achieves a very flat midband gain of approximately two (6 dB) with peaking near roll-off. With proper choice of inductive load, additive-gain cells can be cascaded with overall flat frequency response since the capacitive input of a cell resonates with the inductive output impedance of the preceding stage.

III. INDUCTIVE ELEMENTS

The narrowband amplifier's band-pass characteristics [Fig. 2(a)] and the additive-gain cell's low-pass frequency response [Fig. 2(c)] both depend critically on the resonant interaction between the inductive element and the load capacitance. Therefore, accurate knowledge of the inductor characteristics is imperative.

Sufficiently accurate inductor parameters (including capacitive parasitics) may only be available from

Fig. 3(a) Spiral Inductor
3.25 TURNS

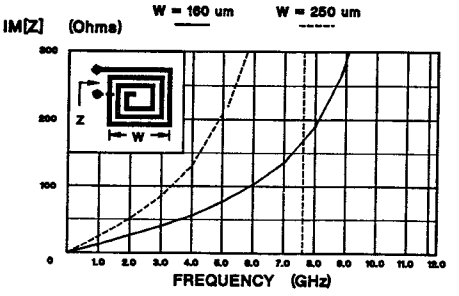
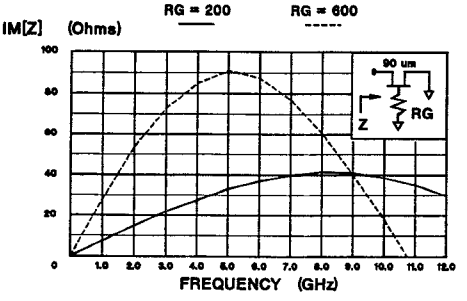


Fig. 3(b) Synthetic Inductor



measured data for a particular process. Shown in Fig. 3(a) is the inductive reactance versus frequency typical of 3.25-turn square spiral inductors with 12 μm trace widths and 3 μm gaps for the process used here. These spirals behave similar to an ideal inductor only up to frequencies approximately one-fifth of the self-resonant frequency. For spirals of the values (typically 4 nH) needed for these designs, a square dimension W=200 μm is required. Allowing for layout clearances to minimize cross-talk, this spiral inductor can approach the size of all other circuit elements combined!

A more compact alternative is the "synthetic inductor," as shown in Fig. 3(b), which is obtained by attaching a gate resistor to a properly biased MESFET. The input impedance of a synthetic inductor is that of an inductor with a series resistor, both of which are frequency dependent.

$$Z=\frac{R_G+\dfrac{g_m}{(\omega C_{gs})^2}}{1+\left(\dfrac{g_m}{\omega C_{gs}}\right)^2}+j\omega\frac{g_m R_G-1}{\omega^2 C_{gs}+\dfrac{g_m^2}{C_{gs}}}=R(\omega)+j\omega L(\omega)$$

The amount of inductance extracted from this device is controlled by the gate resistor (R_G) which must be larger than $1/g_m$ for the reactance to be inductive. A computer simulation [7] of the input reactance, including all the device parasitics, is plotted in Fig. 3(b). It is seen that the reactance of a synthetic inductor resembles an ideal inductor up to frequencies approximately half of its self-resonant frequency. In addition, a 90 μm-wide FET with $R_G=600$ ohms synthesizes more inductance below f=5 GHz ($f_T/3$), than does a spiral with square dimension

W = 160 μm. Choosing a smaller R_G reduces the synthetic inductor's effective inductance, but extends the useful range to higher frequency.

IV. CIRCUIT DESIGN

A transfer curve is generated for the additive-gain cell [7]. The gate-to-source bias of -0.7 volt is applied to two common-source FETs for reduced distortion and power consumption. Two bias resistors, R_1 and R_2 of Fig. 4(a), supply the gate bias voltage and provide the dc feedback [5] to stabilize the FET's bias point from process variations.

A large common-source output driver FET is desired as it is able to drive smaller output resistances and provide higher saturated power output. The size of this output driver, however, is limited because of the maximum power dissipation allowed and the drive capacity of the preceding stage. Simulations [7] indicate that two 150 μm gate-width common-source FETs are sufficient to drive a 350 μm gate-width output driver FET while maintaining a low power dissipation.

The entire circuit is made self-biasing by adjusting the gate-width of the source-follower to 90 μm. The drain current of the 150 μm FET, biased at V_{GS} = -0.7 volt, equals I_{DSS} for the 90 μm source-follower. With this design, all FETs are biased at drain-to-source voltages 3.0 volts.

The synthetic inductor load for this cell is a 90 μm gate-width FET biased at V_{GS} = 0 volt. Simulations show that the control resistor at the gate of the synthetic inductor FET has no effect on the midband gain, but a larger resistor provides more gain peaking just before roll-off. A 500-ohm control resistor gives approximately 1.5 dB of gain peaking for a single stage. An additional 60-ohm resistor is placed in series with the synthetic inductor to obtain desired midband gain. One-stage additive-gain amplifier driving an identical cell indicates a voltage gain of 2.6 (8.2 dB) with 6.5 GHz bandwidth.

For the narrowband design, the common-source FET in the output buffer is converted to a current source of 90 μm gate-width with V_{GS} = 0 volt. For this narrowband "tuned" amplifier, the control resistor of the synthetic inductor FET controls both gain and center frequency. As R_G increases, a higher gain at a lower center frequency is produced. The simulation for a single stage, with a control resistor of 1000 ohms, gives a voltage gain of 2.8 (8.9 dB) and bandwidth of 1.6 GHz centered at 3.5 GHz.

V. MEASURED RESULTS

Three additive-gain cells were cascaded through 4.4 pF thin film capacitors (on-chip) and combined with a 350 μm gate-width output driver FET to form a complete amplifier (Fig.4). In all stages, 550 ohm control resistors were chosen for synthetic inductors to achieve desired gain peaking and bandwidth.

Computer simulation, including all the parasitic capacitances, predicted approximately 26.4 dB of midband gain with 4.5 GHz bandwidth. The measured response, as observed with on-wafer probes and a network analyzer, showed 25.5 dB of midband gain and 4.5 GHz bandwidth. Close agreement to computer simulation is partly due to the simplicity of the additive-gain cell design, which uses FETs of similar widths throughout, and therefore maintains small-signal response and dc bias voltages well, despite process variations.

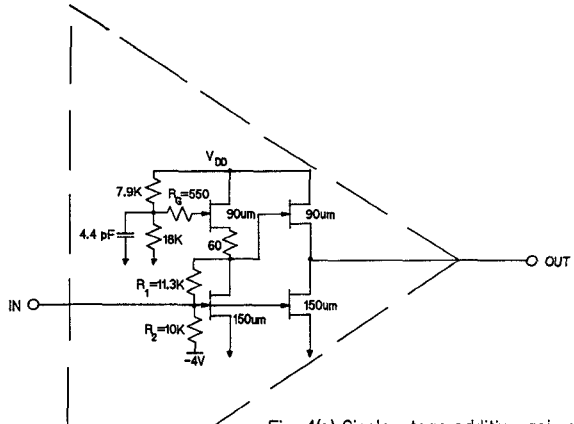


Fig. 4(a) Single-stage additive-gain amplifier

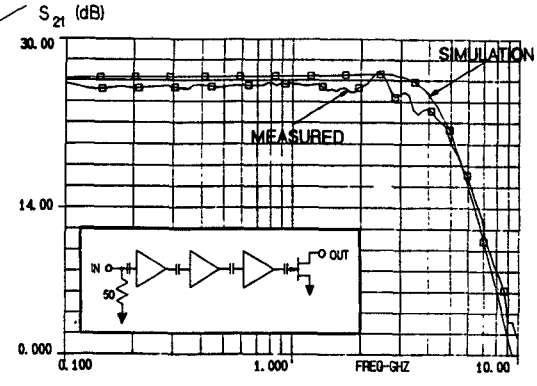
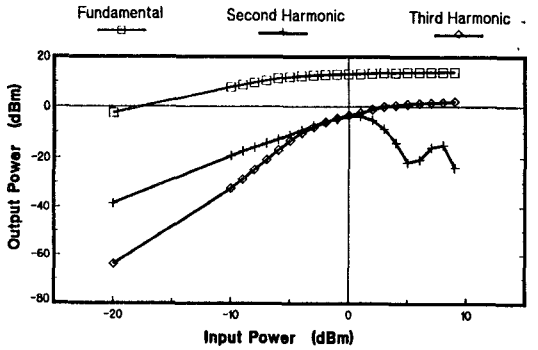


Fig. 4(b) Frequency response of cascaded amplifier

Large-signal measurements made with a microwave spectrum analyzer indicate the 1-dB power compression point at 13 dBm. The amplifier's relative harmonic distortions are shown in Fig. 5. It is noted that the second and third harmonics are well below the fundamental component in the useful range of input power, with second and third harmonic intercepts of 40 dBm and 25 dBm, respectively. The circuit occupies 0.6 X 1.7 mm^2 and consumes 760 mW of power.

The performance of a narrowband amplifier is shown in Fig. 6. Computer simulation indicates a peak gain of 26 dB and a bandwidth of 1.6 GHz centered at 4 GHz. The measurement shows a peak gain of 25 dB and bandwidth of 1.6 GHz at 3.5 GHz. The center frequency of this response can be tuned by varying the synthetic inductor's control resistor, R_G [Fig. 3(b)], which varies the effective inductance.

Fig. 5 Harmonic Distortion



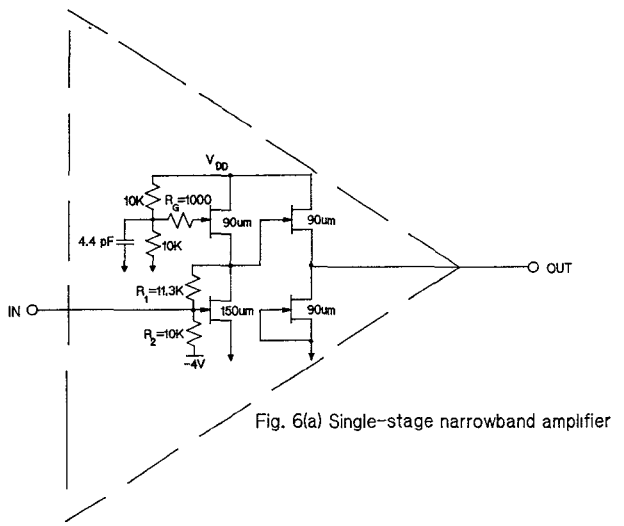


Fig. 6(a) Single-stage narrowband amplifier

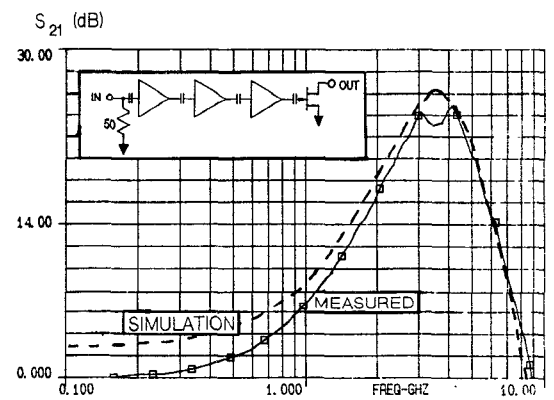


Fig. 6(b) Frequency response of cascaded amplifier

VI. CONCLUSION

Simple GaAs FET cascadable amplifier cells that achieve broadband gain peaking and band-pass frequency response without inductors have been developed. Upper band edges of approaching $f_T/3$ were achieved by integrating a synthetic inductor, consisting of a resistor and a FET, with a common-source amplifier and an output buffer stage. Direct cascading of these cells was demonstrated, with gains >25 dB and upper band edges of 4.5 GHz for three cells with a common-source output driver.

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[7] Simulations were performed with Touchstone(R) and Microwave SPICE(R).

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